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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,851	06/19/2003	Philip B. James-Roxby	X-1279 US	8477

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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,851	JAMES-ROXBY ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-2, 4-6, 8, 10-11 and 13-20* is/are rejected.

7)☒ Claim(s) *3,7,9 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-20 are pending.

Claims 3, 7, 9 and 12 are objected to.

Claims 1-2, 4-6, 8, 10-11 and 13-20 are rejected.

Response to Amendment

2. Applicant's arguments filed 7 October 2005 in response to the office action mailed on 14 July 2005 have been fully considered but they are not persuasive. Therefore the rejections made in the previous office action are maintained, and restated below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-6, 8, 11, 13, 15 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Song (US Patent 5,321,825).

As for claim 1, Song teaches a method for processing data stored in a memory shared among a plurality of processors, comprising:

providing a semaphore associated with a first portion of the memory (Fig. 1, element 62, the ULB lock field contains a bit which is used to indicate if the processor is permitted to access the critical section of the memory -- col.4, lines 60-67);

storing tasks in the first portion of the memory (critical section), the tasks respectively related to information associated with a second portion (lock space) of the memory (Fig. 2, element 130 is the critical section which contains commands (elements 140-6) which operate on data contained in the lock space (element 114) -- col. 5, lines 4-10);

determining a state of the semaphore (col. 8, lines 4-13 – initially the control bit is set to 0 which permits the processor to access the critical memory section);

controlling access among the plurality of processors to the first portion of the memory in response to the state of the semaphore (col. 7, lines 11-15 -- when a processor accesses the critical section of the memory, all remaining processors are locked out); and

executing a task to process at least some of the information within the second portion of the memory in response to a processor of the plurality of processors gaining access to the first portion of the memory (col. 5, lines 4-11 -- the processor will execute instructions from the critical section of the memory which access data operands from the lock space memory).

As for claim 6, Song teaches a method for processing data stored in a memory shared among a plurality of processors, comprising:

storing task data for one or more tasks (Fig. 2, element 130 is the critical section which contains commands (elements 140-6) which operate on data contained in the lock space (element 114) -- col. 5, lines 4-10);

relating each of the one or more tasks to respective one or more data segments stored in a second portion of the memory (col. 5, lines 5-11, data operands are stored in the lock space (e.g. (element 162 of Fig. 2) which are accessed by the instructions stored in the critical memory space));

associating a semaphore with the task data (Fig. 1, element 62, the ULB lock field contains a bit which is used to indicate if the processor is permitted to access the critical section of the memory -- col.4, lines 60-67);

controlling access among the plurality of processors to the task data in response to a state of the semaphore (col. 7, lines 11-15 -- when a processor accesses the critical section of the memory, all remaining processors are locked out); and

executing a task of the one or more tasks to process a respective data segment in response to a processor of the plurality of processors gaining access to the task data (col. 5, lines 4-11 -- the processor will execute instructions from the critical section of the memory which access data operands from the lock space memory).

As for claim 2 and 8, Song further discloses the method wherein the controlling comprises:

allowing one of the plurality of processors to access the first portion of the memory responsive to the semaphore having a first state value (col. 8, lines 49-55 – processor (element 12) is permitted to execute within the critical section as it is set to 0); and

blocking access to all of the plurality of processors to the first portion of the memory responsive to the semaphore having a second state value (col. 8, lines 53-57 – the other processors are blocked as the control bit used to determine their access control has been set to 1 (col. 8, lines 45-50)).

As for claim 4, Song further teaches coupling the semaphore to a bus shared by each of the plurality of processors (Fig. 1, element 18 discloses a bus connecting the processors to the shared memory and the semaphore used to determine control access to the critical section of the memory.

As for claim 5, Song teaches the method of claim 1, wherein the storing comprises:

initializing state of the semaphore to allow access to the first portion of the memory (col. 8, lines 4-8, the initial state is set to 0); and

receiving tasks to be executed by the processor of the plurality of processors (col. 5, lines 4-11 -- the processors obtain and execute

instructions from the critical section of the memory which access data operands from the lock space memory).

As for claim 11, Song teaches classifying each of the tasks with an identifier indicative of the task type (lock, unlock, read-lock, write-lock) in Fig. 2, elements 150, 152, 154 and 156 within the critical section element 132.

As for claims 13 and 15, Song discloses a system and an apparatus for processing data stored in a memory shared among a plurality of processors, comprising:

a memory (Fig. 1, element 16);

and an integrated circuit including:

a semaphore circuit associated with a first portion of the memory, the semaphore circuit coupled to a bus shared by each of the plurality of processors (Fig. 1, element 62, the ULB lock field contains a bit which is used to indicate if the processor is permitted to access the critical section of the memory, which is further connected to the bus (element 18) -- col.4, lines 60-67. Note the buffer which contains the bit used as a semaphore in Song's teachings can be part of integrated circuit common with the processors, therefore it itself must contain logic (i.e. circuitry) and can not be limited to a strictly software implementation – col. 9, lines 41-47);

means for storing tasks in the first portion of the memory, the tasks respectively related to data segments stored in a second portion of the memory (col. 5, lines 5-11, data operands are stored in the lock space (e.g. (element 162 of Fig. 2) which accessed by the instructions stored in the critical memory space);

means for controlling access among the plurality of processors to the first portion of the memory in response to a state of the semaphore circuit (col. 7, lines 11-15 -- when a processor accesses the critical section of the memory, all remaining processors are locked out); and

means for executing a task to process a data segment in response to a processor of the plurality of processors gaining acçess to the first portion of the memory (col. 5, lines 4-11 -- the processor will execute instructions from the critical section of the memory which access data operands from the lock space memory once permission is granted through the LUB lock field).

As for claim 20, Song discloses the system of claim 15, wherein the means for controlling comprises:

allowing one of the plurality of processors to access the first portion of the memory responsive to the semaphore having a first state value (col. 8, lines 49-55 – processor (element 12) is permitted to execute within the critical section as it is set to 0); and

blocking access to all of the plurality of processors to the first portion of the memory responsive to the semaphore having a second state value (col. 8, lines 53-57 – the other processors are blocked as the control bit used to determine their access control has been set to 1 (col. 8, lines 45-50)).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song as applied to claim 15 above, and further in view of Trimberger (US Patent 6,573,748 B1).

As for claims 16 and 18, though Song teaches his system as being integrated together within a single integrated circuit (hereinafter IC) in col. 9, lines 41-46, he fails to further define the IC as a programmable logic device which is configured using programmable logic blocks.

Trimberger however discloses a programmable logic device, which is configurable (i.e. used as a processor in col. 1, lines 59-61) to increase the chip's versatility. Trimberger's programmable logic device (hereinafter PLD) utilizes an

array of programmable logic blocks for the purposes of configuring the device (col. 1, lines 14-21). As Trimberger discloses, a PLD has many advantages because they are less expensive, and require less time to implement than semi-custom and fully custom ICs.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Song to allow further define his IC as an PLD IC in order to capitalize on the programmable features as disclosed by Trimberger. As taught by Trimberger, the increased programmability would help Song realize both decrease cost and implementation time.

As for claim 17, Song discloses each of the unique processors as being embedded within the IC (col. 9, lines 41-44).

5. Claims 10, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song as applied to claims 6, 13, and 15 above, and further in view of Aucsmith et al. (hereinafter Aucsmith US Patent 6,243,793 B1).

As for claims 14 and 19, though Song fails to teach providing an additional memory respectively coupled to each of the plurality of processors, Aucsmith teaches a system for arbitrating access to a shared memory area which contains an additional memory, capable of storing program data to be executed by the processors (Fig. 2, element 103 illustrates a mass storage device that is connected to each of the two processors – col. 4, lines 12-18 the mass storage device provides information and data to the external memory which is used by the processors (i.e. element 104 in Fig. 2)). It would have been obvious to one of

ordinary skill in the art at the time of the invention for Song to further add an external memory to his processing system. By doing so, his system would benefit from additional storage area used to help coordinate memory access between the processors necessary to allow a plurality of processors operate on a shared memory as taught Aucsmith (col. 1, lines 15-21).

As for claim 10, though Song fails to the method of claim 6 further comprising storing an identifier for the processor that executed the task, Aucsmith teaches a system for arbitrating access to a shared memory area with the use of an indicator (memory marker unit—Fig. 1, element 107) which is contained within the shared memory for the purpose of indicating which processor executed a task or process (col. 4, lines 43-53).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Song to further include the memory marker in his system in order to track the historical information of the tasks executed by the processors. By doing so, Song's system would benefit by allowing the next processor to access shared memory to know which processor performed the previous tasks, allowing the processors to more effectively communicate with each other as discussed by Aucsmith in col. 1 lines 37-49.

Allowable Subject Matter

6. Claims 3, 7, 9 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicants' arguments filed 7 October 2005 with respect to the rejections under 35 USC 102 and 35 USC 103 have been fully considered but they are not persuasive.

8. With respect to the argument under the heading "Rejection Of Claims Under 35 U.S.C. § 102", Applicants assert that claims 1, 6, 13 and 15 overcome Examiner's cited art (herein Song) since Song does not teach or suggest providing a semaphore and "controlling access among the plurality of processors to the first portion of the memory in response to the state of the semaphore". Further, Applicants assert that Song does not teach or suggest controlling access to a shared memory among multiple processors based on the status of a single semaphore or lock buffer ("the semaphore"). Applicants cite the same justification for the allowance of claims 6, 13 and 15 based on the similar recitation of "a semaphore [or semaphore circuit] to control access among the plurality of processors to the first potion of the memory in response to a state of the semaphore circuit". Examiner finds that Applicants' arguments are not persuasive for the following reasons:

Claim 1 (and similarly clams 6, 13 and 15) recites the limitation of "controlling access among the plurality of processors to the first portion of the

memory in response to the state of the semaphore" (or a similar variation thereof for claims 6, 13 and 15). Examiner has shown by citing col. 7, lines 11-15 and col. 8, lines 4-13 (pages 2-3 of the previous correspondence) that Song in fact teaches using a (emphasis added) semaphore to "control access among [a] plurality of processors to the first portion of the memory in response to the state of the semaphore". By setting the semaphore (i.e. ULB lock), Song's system is controlling the access of one processor (by granting it access) to the first portion of the memory, and likewise controlling access (in this instance, blocking the access) to the first portion of the memory of the remaining processors. The fact that Song teaches using multiple lock buffers immaterial, as one (emphasis added) semaphore has the ability to control the access of all processors (either by granting, or denying access) to the first portion of memory. Further, though Song teaches the processors accessing non-critical sections during this "locking" time period, they cannot access an instruction that requires the use of the lock space (i.e. areas contained within the critical sections). Note the Examiner originally labeled the critical section of the memory as the "first section of the memory", therefore this is consistent with the original argument set forth in the previous correspondence.

As for claims 2, 4-5, 8, 11 and 20, Applicants' argument that these claims are allowable because they depend on either 1 or 15 (directly or indirectly) is rendered moot as claims 1 and 15 currently stand rejected under 35 U.S.C. 102(b).

9. With respect to the argument under the heading "Rejection Of Claims Under 35 U.S.C. § 103", Applicants assert that Song does not teach or suggest a semaphore circuit and a "means for controlling access among the plurality of processors to the first portion of the memory in response to a state of the semaphore circuit" as recited in claim 15. Applicant's arguments are not persuasive, therefore the Examiner maintains the rejections under the heading 35 U.S.C 103 for the very reasons stated above (under section eight of this correspondence).

10. With respect to the argument under the heading "Objections", the objections to these claims are maintained as the Examiner asserts that the rejection of the independent claims (1, 6, 13, 15) has been shown to be proper.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vartti et al. (US Patent 5,678,026) disclose a Multi-processor data processing system with control for granting multiple storage locks in parallel and parallel lock priority and second level cache priority queues.

Barriuso et al. (US Patent 5,535,365) disclose a method and apparatus for locking shared memory locations in multiprocessing systems.

Vartti et al. (WO 02/054250A2) disclose a method and apparatus for controlling memory storage locks based on cache line ownership.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

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SUPERVISORY PATENT EXAMINER